IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:

Fitzgerald, et al.

GROUP:

2823

JRADENSERIAL NO:

10/603,850

EXAMINER:

Belur V. Keshava

FILED:

06/25/2003

Date of mailing

of Notice of

FOR: COPLANAR INTEGRATION OF

Allowance:

3/28/2005

LATTICE-MISMATCHED SEMICONDUCTOR

WITH SILICON VIA WAFER BONDING VIRTUAL

SUBSTRATES

Mail Stop Issue Fee Assistant Commissioner of Patents P.O. Box 1450, Alexandria, VA 22313-1450

Attn: Official Draftsman

TRANSMITTAL OF FORMAL DRAWINGS

Applicant submits herewith new drawing(s) for this application. Attached please find twelve (12) sheets of formal drawings for this application.

The three month period of response set in the Notice of Allowability (PTOL 37) expires on June 28, 2005 and this submission is on or before this expiry date.

Respectfully submitted,

Matthew E. Connors Registration No. 33,298 Gauthier & Connors LLP 225 Franklin Street, Suite 3300 Boston, Massachusetts 02110

Telephone: (617) 426-9180

Extension 112

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22312-1450, Mail Stop: Issue Fee.

Elizabeth M. Ball

Date: $(\rho - 23 - 05)$